UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,395	08/14/2008	Hien Boon Tan	Q78657	3868

23373 7590 09/30/2011

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
GOODWIN, DAVID J	
ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
09/30/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

sughrue@sughrue.com
PPROCESSING@SUGHRUE.COM
USPTO@SUGHRUE.COM

Office Action Summary	Application No.	Applicant(s)	
	10/581,395	TAN ET AL.	
	Examiner	Art Unit	
	DAVID GOODWIN	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *5-9 and 13-21* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *5-9 and 13-21* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 20 and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. Claims 20 and 21 recite the limitation "only said conductive bumps provide said standoff between said chip and said substrate" in lines 1 and 2.

3. The specification as filed does not support this because the specification teaches that the standoff between the substrate and the chip comprises the void where the underfill material will subsequently be provided or the underfill material. Therefore the applicant does not teach a standoff that consists only of conductive bump material.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5, 9, 13, 14, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6946732) in view of Lee (US 7161237).

3. Regarding claim 5.

4. Akram teaches a method of producing a chip scale package comprising only one integrated circuit chip. Said package comprises mounting an integrated chip (10) on a substrate (20). Each integrated chip (9) comprising a plurality of bond pads (12). Each of said bond pads is aligned in a central row. A plurality of conductive bumps (30) formed on the plurality of bond pads (12), wherein said bumps (30) align with corresponding solder pad openings (40) on an upper surface of the substrate (20) and wherein the standoff between said chip (10) and said substrate (20) is provided mainly by conductive bumps (30). Reflowing the integrated chip (10) of each array, thereby melting the bumps and establishing a conductive joint between the integrated circuit chip (10) and the substrate (20) (fig 8, 9) (column 8 line 40-column 10 line 40).

5. Akram does not teach that each bond pad is aligned in only a central row.

6. Akram teaches an embodiment wherein each bond pad (202) of the chip (200) is aligned in only a central row.

7. It would have been obvious to one of ordinary skill in the art to provide only a single row of bond pads in order to provide only the required connections. In re Kuhle 188 USPQ 7.

8. Akram does not teach under filling and dicing the structure.

9. Lee teaches a method of producing chip scale packages. Said method comprises mounting an array (250) of integrated circuit chips on a substrate (210). Each integrated circuit chip comprises a plurality of centrally located bond pads (258). A plurality of conductive bumps (256) formed on the plurality of bond pads (256), wherein said bumps align with corresponding solder pad openings (220)on an upper

surface of the substrate (210) wherein the standoff between the chip and the substrate is provided mainly by the conductive bumps. Under fill encapsulating with dielectric filler (column 16 lines 55-60). Dicing the array, joined to the substrate, into individual chip scale packages each comprising one integrated circuit chip (column 15 line 40-column 16 line 20) (fig 13a,b)

10. It would have been obvious to one of ordinary skill in the art to encapsulate and dice the chips joined to the substrate in order provide multiple individual packages.

11. Regarding claim 9.

12. Lee teaches forming, before dicing the array into individual chip packages, solder balls (262) conductively connected to the bumps on the under surface of the substrate (210) (column 16 lines 15-30) (fig 13a,b)

13. Regarding claim 13

14. Lee teaches that the array (25) provided comprises a wafer portion having multiple semiconductor dice (column 15 lines50-60).

15. Lee does not teach how a portion of a wafer is obtained.

16. Lee teaches that a semiconductor wafer can be portioned by dicing (column 16 lines10-20).

17. It would have been obvious to one of ordinary skill in the art to porion a wafer by dicing to obtain an array in order cleanly separate the portion from the remaining wafer portion.

18. Regarding claim 14.

19. Akram teaches a method of producing a chip scale package comprising only one integrated circuit chip. Said method comprises mounting an integrated chip (10) on a substrate (20). Each integrated chip (9) comprising a plurality of bond pads (12). Each of said bond pads is aligned in only a central plurality of rows. A plurality of conductive bumps (30) formed on the plurality of bond pads (12), wherein said bumps (30) align with corresponding solder pad openings (40) on an upper surface of the substrate (20) and wherein the standoff between said chip (10) and said substrate (20) is provided mainly by conductive bumps (30). Reflowing the integrated chip (10) of each array, thereby melting the bumps and establishing a conductive joint between the integrated circuit chip (10) and the substrate (20) (fig 8, 9) (column 8 line 40-column 10 line 40).

20. Lee teaches a method of producing chip scale packages. Said method comprises mounting an array (250) of integrated circuit chips on a substrate (210). Each integrated circuit chip comprises a plurality of centrally located bond pads (258). A plurality of conductive bumps (256) formed on the plurality of bond pads (256), wherein said bumps align with corresponding solder pad openings (220)on an upper surface of the substrate (210) wherein the standoff between the chip and the substrate is provided mainly by the conductive bumps. Under fill encapsulating with dielectric filler (column 16 lines 55-60). Dicing the array, joined to the substrate, into individual chip scale packages each comprising one integrated circuit chip (column 15 line 40-column 16 line 20) (fig 13a,b)

21. It would have been obvious to one of ordinary skill in the art to encapsulate and dice the chips joined to the substrate in order provide individual packages.

22. Regarding claim 18

23. Lee teaches forming, before dicing the array into individual chip packages, solder balls (262) conductively connected to the bumps on the under surface of the substrate (210) (column 16 lines 15-30) (fig 13a,b)

24. Regarding claim 19

25. Lee teaches that the array (25) provided comprises a wafer portion having multiple semiconductor dice (column 15 lines50-60).

26. Lee does not teach how a portion of a wafer is obtained.

27. Lee teaches that a semiconductor wafer can be portioned by dicing (column 16 lines10-20).

28. It would have been obvious to one of ordinary skill in the art to porion a wafer by dicing to obtain an array in order cleanly separate the portion from the remaining wafer portion.

29. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6946732) in view of Lee (US 7161237) as applied to claim 5 and further in view of Qi (US 6774497).

30. Regarding claim 6.

31. Qi teaches, prior to mounting, dipping each array in flux material such that flux (124) material adheres to the bumps (120) (fig 1). Wherein each array is mounted on a substrate the flux material adheres the bumps to the solder pad openings (242) (fig 2a) (column 5 lines 20-25).

32. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6946732) in view of Lee (US 7161237) (US 6181569) in view of Qi (US 6774497) as applied to claim 6 and further in view of Lance (US 5697148)

1. Regarding claim 7

2. Akram in view of Lee in view of Qi teaches elements of the claimed invention above.

3. Akram in view of Lee in view of Qi does not teach cleaning the flux from the device

4. Lance teaches cleaning the flux from the device (column 1 lines 20-35).

5. It would have been obvious to on e of ordinary skill in the art to clean the fluc from the device in order to prevent corrosion.

6. Regarding claim 8

7. Akram in view of Lee in view of Qi teaches elements of the claimed invention above.

8. Akram in view of Lee in view of Qi does not teach injecting the encapsulant.

9. Lance teaches injecting the encapsulant (22) between the chip (12) and the substrate (14).

10. It would have been obvious to one of ordinary skill in the art to inject the encapsulant in order to alleviate problems of thermal mismatch.

33. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6946732) in view of Lee (US 7161237) as applied to claim 14 and further in view of Qi (US 6774497).

11. Regarding claim 15.

12. Akram in view of Lee teaches elements of the claimed invention above

13. Akram in view of Lee does not teach dipping in flux.

14. Qi teaches, prior to mounting, dipping each array in flux material such that flux (124) material adheres to the bumps (120) (fig 1). Wherein each array is mounted on a substrate the flux material adheres the bumps to the solder pad openings (242) (fig 2a) (column 5 lines 20-25).

34. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram (US 6946732) in view of Lee (US 7161237) in view of Qi (US 6774497) as applied to claim 15 and further in view of Lance (US 5697148)

35. Regarding claim 16

36. Akram in view of Lee in view of Qi teaches elements of the claimed invention above.

37. Akram in view of Lee in view of Qi does not teach cleaning the flux from the device

38. Lance teaches cleaning the flux from the device (column 1 lines 20-35).

39. It would have been obvious to on e of ordinary skill in the art to clean the flux from the device in order to prevent corrosion.

40. Regarding claim 17

41. Akram in view of Lee in view of Qi teaches elements of the claimed invention above.

42. Akram in view of Lee in view of Qi does not teach injecting the encapsulant.

43. Lance teaches injecting the encapsulant (22) between the chip (12) and the substrate (14).

44. It would have been obvious to one of ordinary skill in the art to inject the encapsulant in order to alleviate problems of thermal mismatch.

Response to Arguments

45. Applicant's arguments with respect to claims 5 through 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID GOODWIN whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571)272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Djg

/STEVEN LOKE/
Supervisory Patent Examiner, Art Unit 2818